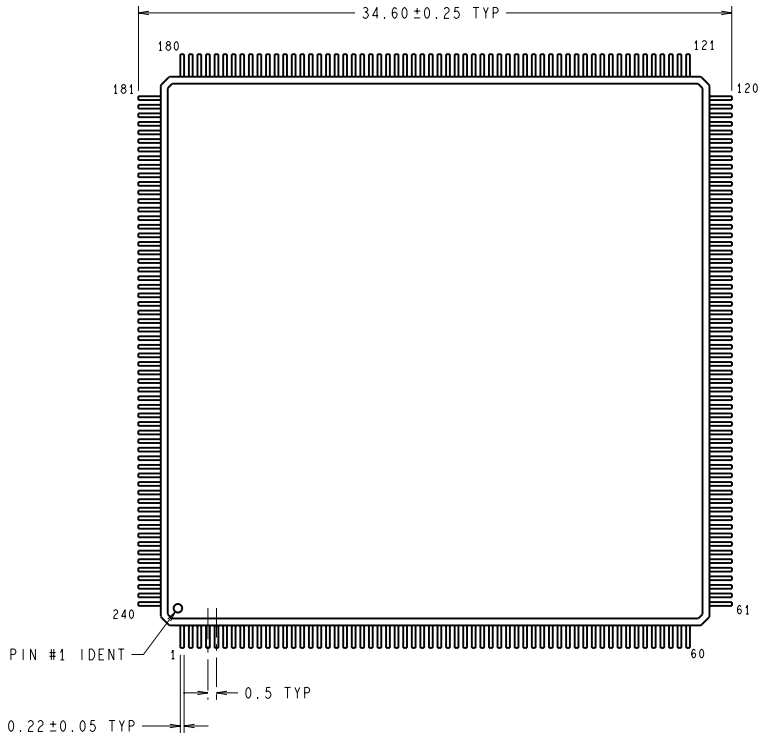
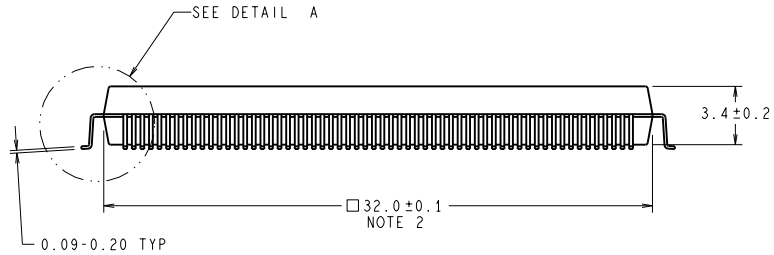
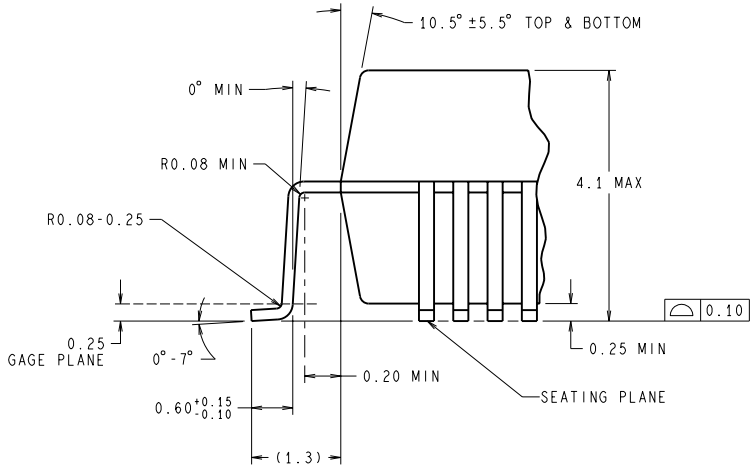
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL.	11009	07/26/95	DEG/







DETAIL A
TYP, SCALE: 20X

DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
   MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
3. REFERENCE JEDEC REGISTRATION MO-143, VARIATION GA,
   DATED MAR/93.

APPROVALS	DATE
DRAWN: D.E.Grady	07/26/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

PQFP, JEDEC METRIC,
32 X 32 X 3.4mm,
240 LEAD

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-VWA240A	A

DO NOT SCALE DRAWING | SHEET 1 of 1