4.5.9 – 144 PIN DDR SGRAM SO–DIMM FAMILY

GENERAL FEATURES

- 144-pin small outline dual in line memory module (SO-DIMM)
- 64-bit data bus with no ECC and no parity
- Module capacity ranges from 1 MB to 8 MB
- Supports 8 Mb and 16 Mb double data rate (DDR) SGRAMs
- Dual supply 3.3 V and 2.5 V
- 2.5 V DDR I/O Class B on single data rate (SDR) signals
- 2.5 V DDR I/O Class A on double data rate signals
- Similar to existing SDR SO-DIMM

CAPACITY—Module capacity ranges from 1 MB to 8 MB

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT without PARITY
—64 BIT without PARITY

CONFIGURATION—4 Different Configurations are defined using X32 SGRAM memories in 1 and 2 bank configurations.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature (optional) that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

HARDWARE FEATURES—Physical layout parameters and terminating resistors are given to optimize the speed characteristics of the module. The key has been located at pin 50 and is different from the other 144 P SO–DIMM packages.

LOGIC iNTERFACE LEVELS—The interface signals fall into three classes as defined in Tables 1 & 2
Single Data Rate Signals (SDR)
Double Data Rate Signals (DDR)
Serial EEPROM signals (EEPROM)

POWER SUPPLIES—There are 3 power supplies as defined in Tables 1 & 2
VDD,
VCCQ
VDDSPD

PIN ASSIGNMENTS —Figs. 4.5.9–A & 4.5.9–B

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE with the Key at pin 50.

Clock Net Routing —Fig. 4.5.9–C

512K X 1 Bank X 32 Block Diagram (1 bank of 512K X 32) — Fig. 4.5.9–D

512K X 1 Bank X 64 Block Diagram (1 bank of 512K X 64) — Fig. 4.5.9–E

512K X 2 BanksX 32 Block Diagram (2 banks of 512K X 32) — Fig. 4.5.9–F

1024K X 2 Banks X 32 Block Diagram (2 banks of 1024K X 32) — Fig. 4.5.9–G

Changes From Single Data Rate SO-DIMM

Single Data Rate	Double Data Rate
Single 3.3 V supply VDD (18 pins)	3.3 V VDD (4 pins), 2.5 V VDDQ (15 pins), VDDSPD (1 pin)
All signals 3.3 V LVTTL	DDR signals are 2.5 V DDR I/O Class A, SDR signals are 2.5 V DDR I/O Class B
Single ended clock, no return data strobe	Differential clock with return data strobe
Clock and data loading not matched	Clock and data loading matched
Clock 0 supplied to both SGRAMs on top side. Clock 1 to both SGRAMs on bottom	Clock 0 applied to SGRAMs on DQ(31:0), Clock 1 to SGRAMs on DQ(63:32)
Few termination resistors required	Series termination on all DDR signals
PQFP or TQFP SGRAM packages	LQFP SGRAM packages
3.3 V Serial Presence Detect (SPD) EEPROM optional	SPD required, with separate supply voltage pin
Pulldown resistors indicate module speed	Module speed parameters stored in SPD
Some references to TSOP options	No TSOP references

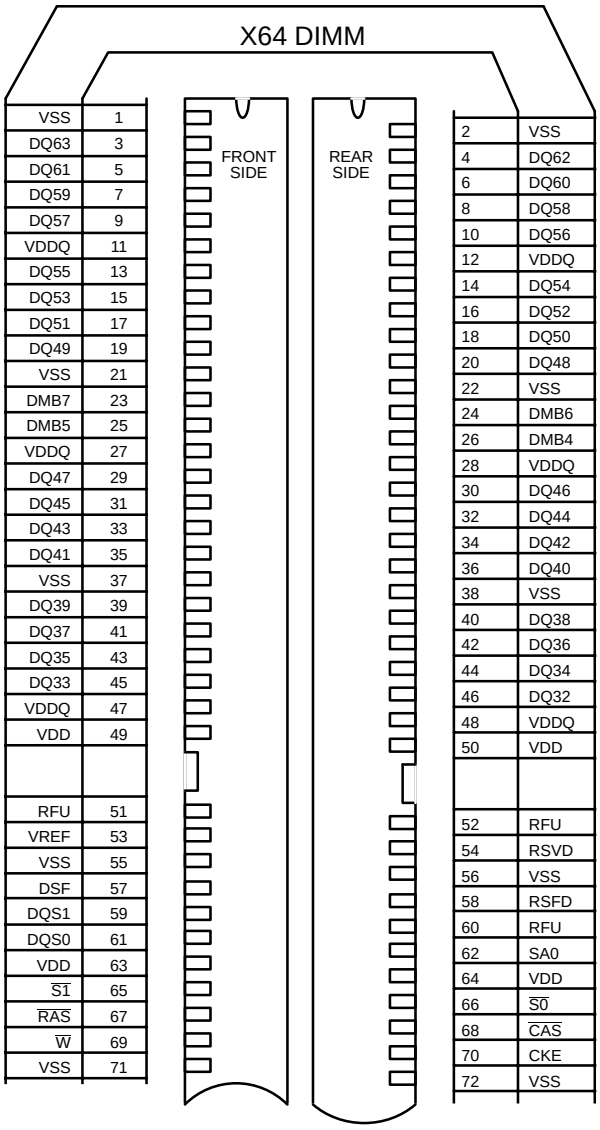

FIGURE 4.5.9–A
144 Pin X32 & X64 DDR SGRAM SO–DIMM, PIN ASSIGNMENTS UPPER HALF

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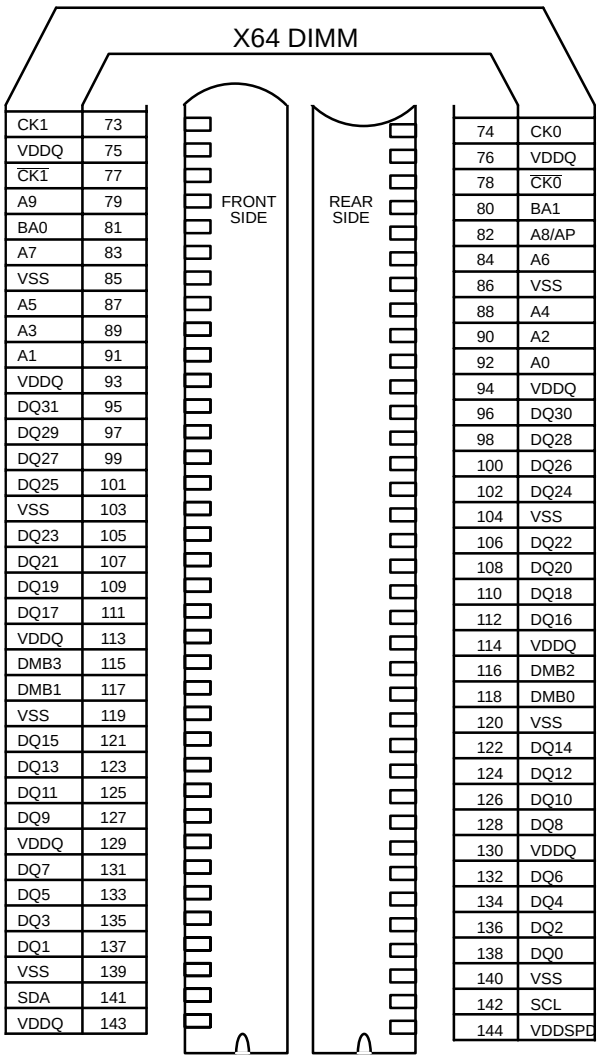


FIGURE 4.5.9–B
144 PIN X32 & X64 DDR SGRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

SGRAM Single Data Rate	SGRAM Double Data Rate	Serial EEPROM	Power Supply
A(9:0)	CK(1:0)	SA0	VDD
BA(1:0)	$\overline{\text{CK}}$(1:0)	SCL	VDDSPD
CAS	DMB(7:0)	SDA	VDDQ
CKE	DQ(63:0)		VREF
DSF	DQS(1:0)		VSS
RAS			
$\overline{\text{S}}$(1:0)			
WE			

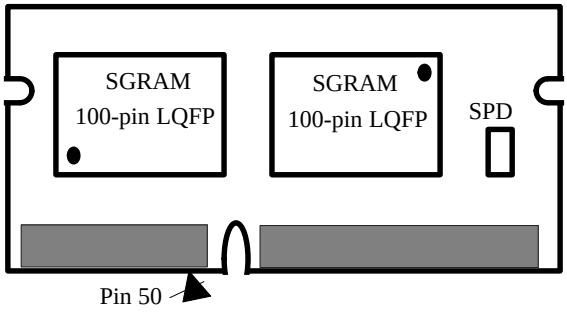
Table 1, Signal and Power Supply Types

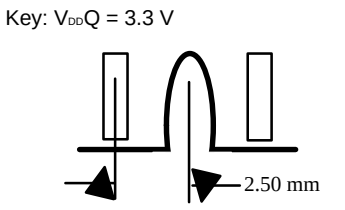
Signal/Supply Name	Characteristic
SDR Si gnal	2.5 V DDR Class B
DDR Signal	2.5 V DDR Class A
EEPROM Signal	3.3 V LVTTL
VDD	3.3 V
VDDQ	2.5 V
VDDSPD	As Needed for EEPROM
VREF	As Needed for SGRAM

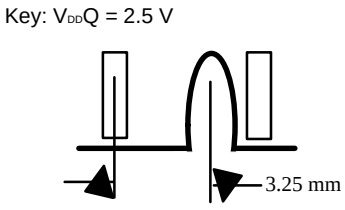
Table 2, Signal and Power Supply Characteristics

Mechanical Outline

- Dimensions: 67.6 mm length, 25.4-50.8 mm height, 1 mm PCB thickness
- Key for $V_{DD}Q$ = 3.3 V or $V_{DD}Q$ = 2.5 V.







Configuration

Graphic controllers can determine the module capabilities by interrogating the Serial Presence Detect EEPROM

Serial Presence Detect EEPROM

The SPD EEPROM is required on this module. Contents are defined in a Sec. 4.1. The SPD uses a separate pin, VDDSPD, as its supply voltage and may be powered separately from the rest of the module for reading or programming.

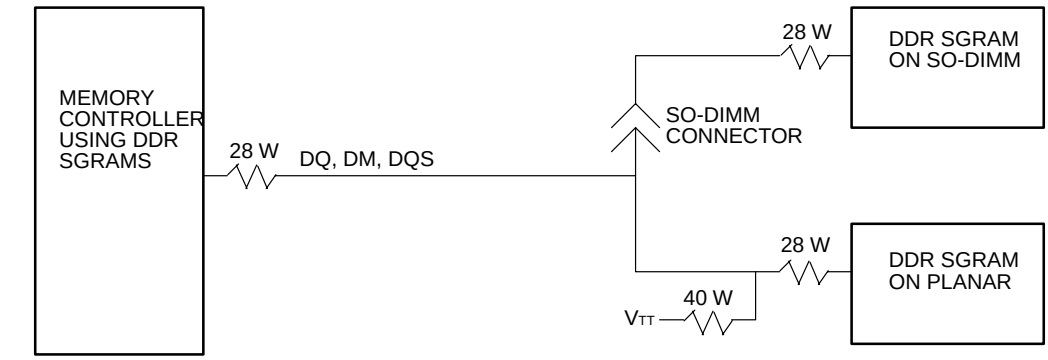
Electrical Characteristics

The primary target design for this module is a planar design with two SGRAMs soldered to the planar, plus an SO-DIMM connector for an optional upgrade with two SGRAMs on the module. This yields a 64-bit bus with 4 MB expandable to 8 MB using standard 16 Mb SGRAMs. 8 Mb SGRAMs can be used for half-capacity configurations, i.e. 2-4 MB.

A secondary design target for this module is a planar design with four SGRAMS soldered to the planar, plus the SO-DIMM connector for an optional upgrade with an SO-DIMM with four SGRAMs on it. These designs place more loads on the double data rate lines and may operate at a somewhat lower speed, depending on planar layout considerations.

For designs in which a 32-bit interface is sufficient, this specification defines an option to use half of the SO-DIMM data bus.

When two SGRAMs are on the planar or two SGRAMs are on the module, they are assumed to both be soldered to the top side of the planar or module, respectively. When four SGRAMs are on the planar or four SGRAMs are on the module, it is assumed that two are on the top side and two are on the bottom side of the planar or module, respectively.The recommended termination scheme for this application is to locate 28 Ω series termination near each component on these double data rate lines: DM, DQ, DQS. In addition, each of these lines is to have a 40 Ω parallel termination resistor to V_{TT} located near the series termination resistor on the planar. The length of all DQ and DM lines should be as similar as possible to minimize skew, and should be the same to the SGRAM on the planar and to the SGRAM on the SO-DIMM. A DQS line should be as long as the longest data line from the associated 32 bit DQ bus.



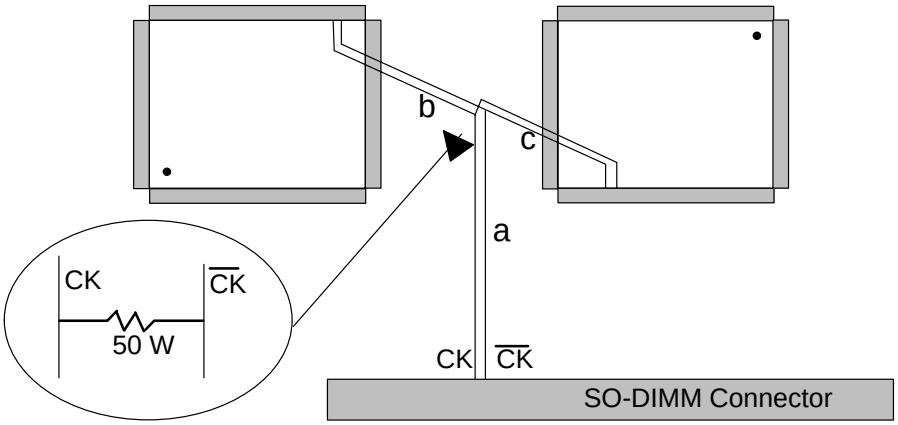
Designing Single/Double Data Rate Systems

The design of the DDR SO-DIMM is intentionally as similar as possible to the SDR SO-DIMM in order to ease the design of systems that can accept both modules. The following planar options can be stuffed at late stages of manufacturing to configure a board for either SDR or DDR.

DDR	SDR
Jumper VDDQ to 2.5 V	Jumper VDDQ to 3.3 V
Use DQS for read clocking	Use echo clock with serpentine on planar
Stuff 28 Ω series termination	Stuff 0 Ω series termination
Stuff 40 Ω parallel termination	Do not stuff parallel termination
Supply both CK0 and CK1	If the design has one clock, short CK0 to CK1
0 Ω resistors installed near the controller on /CK(1:0)	Do not stuff 0 Ω resistors on /CK(1:0)

Clock Net Wiring

Clock loading is two loads per line, maximum. Routing should be performed using a T-topology, as shown below. The CK and $\overline{CK}$ lines should be routed side by side, terminated together with a 50 Ω resistor near the T.



The following table lists the allowable stub lengths for the clock routing:

Parameters	Min	Max	Units
a	75	150	ps
b	0	115	ps
c	0	115	ps
b+c	175	325	ps
Total length (clock)	0	325	ps
Total length (chip select)	0	365	ps

FIGURE 4.5.9–C
CLOCK NET WIRING

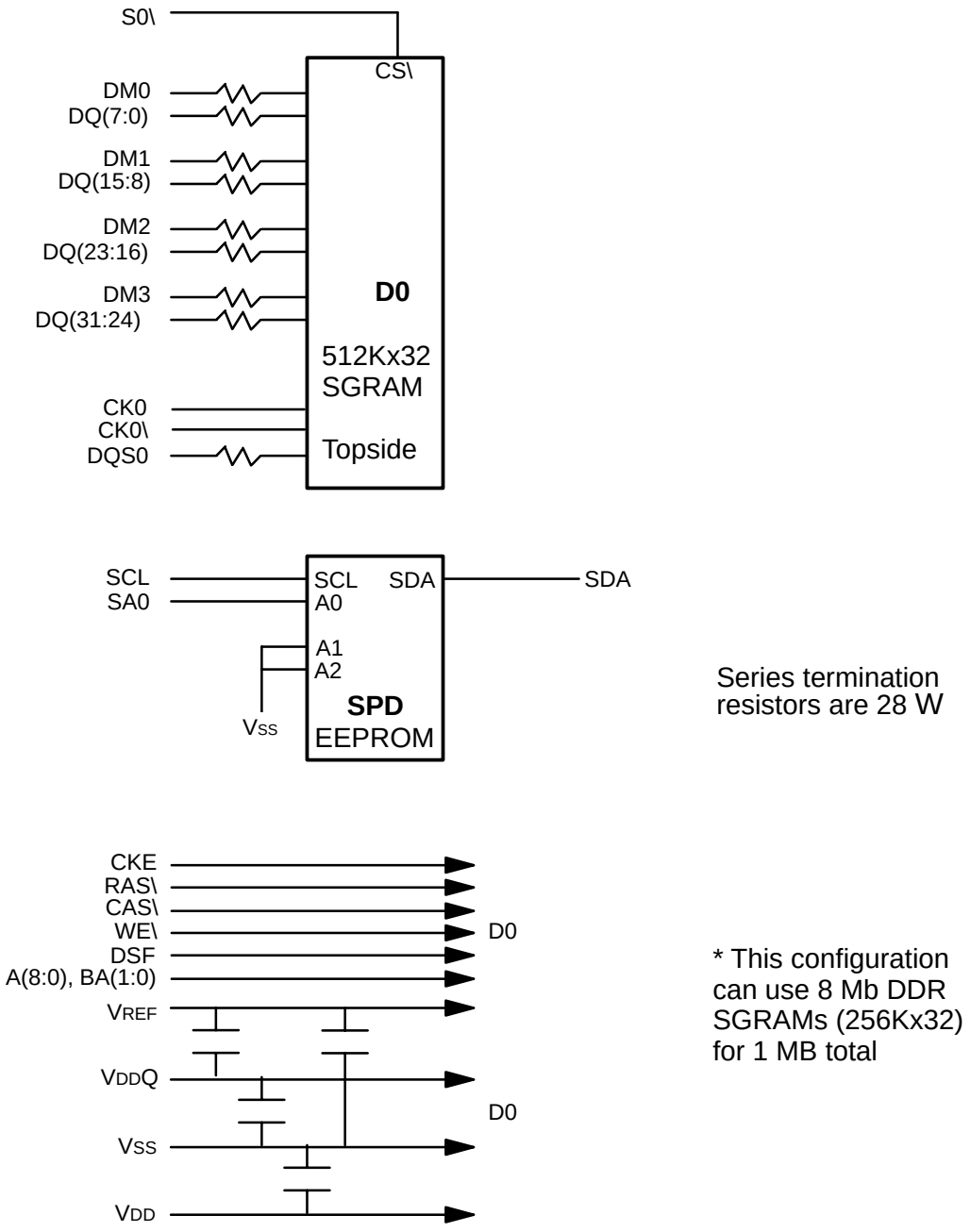


FIGURE 4.5.9–D
144 Pin, 512K X 1 Bank X 32 Configuration (2 MB)*

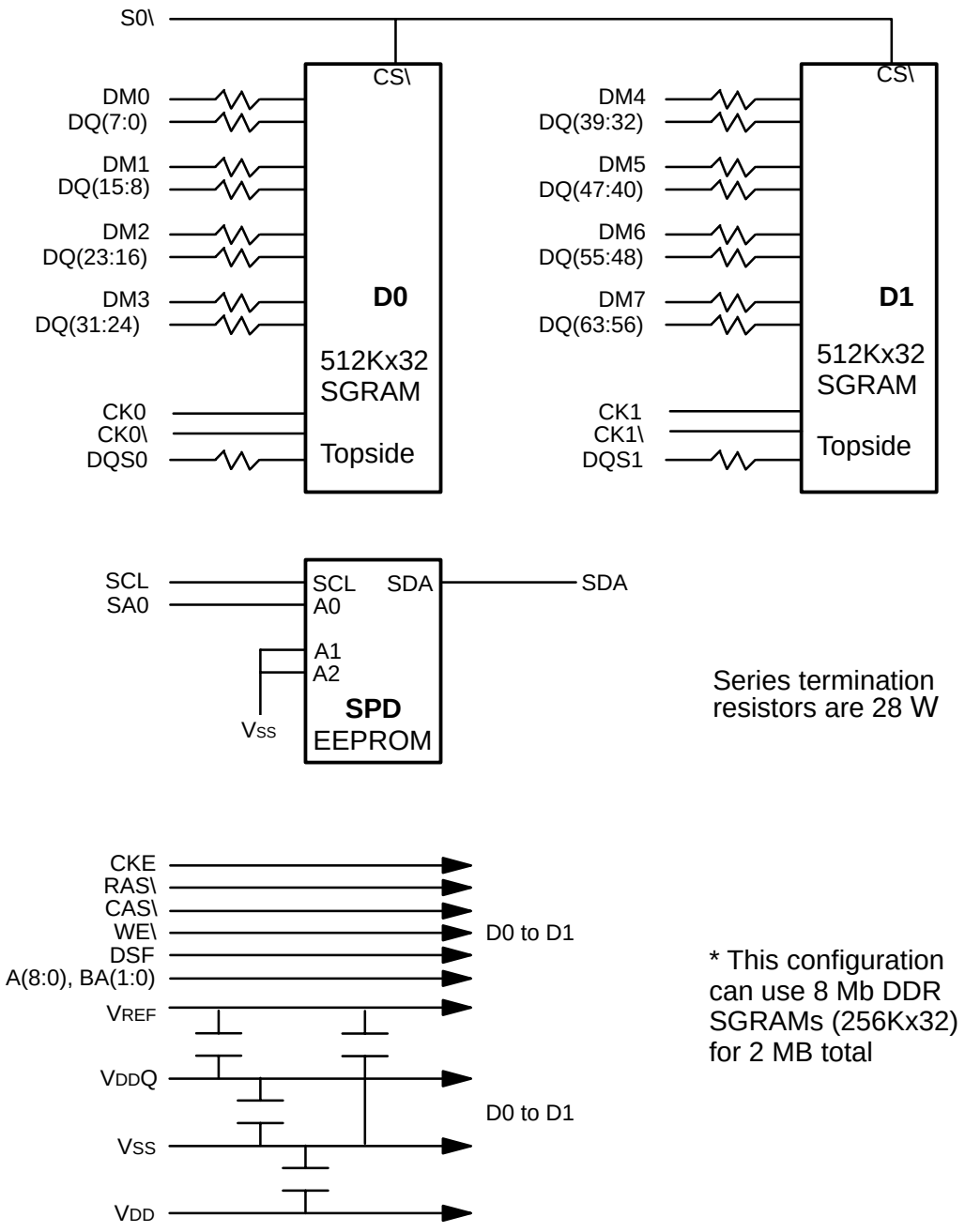


FIGURE 4.5.9–E
144 Pin, 512K x 1 Bank x 64 Configuration (4 MB)*

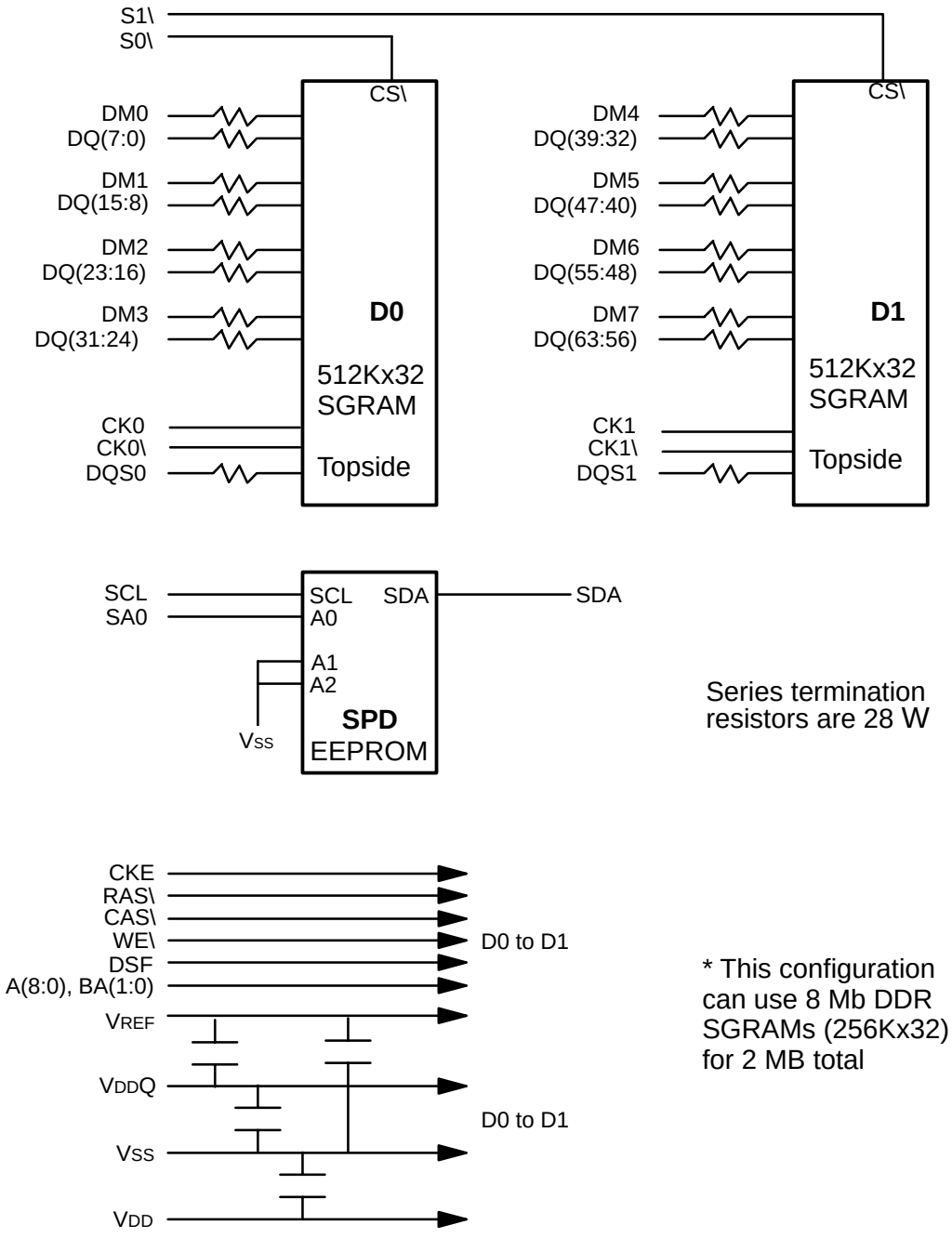
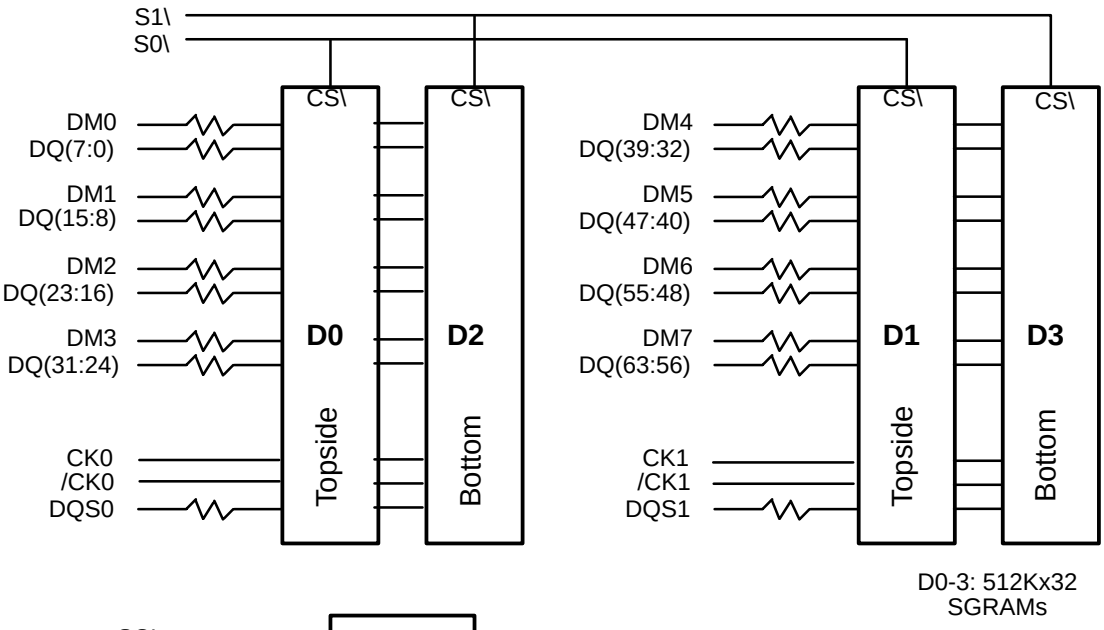
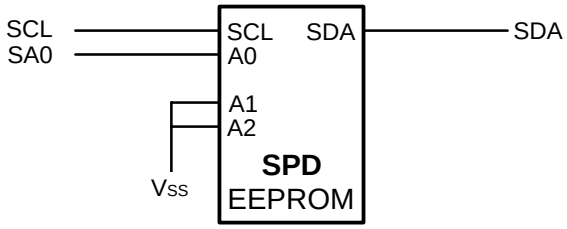
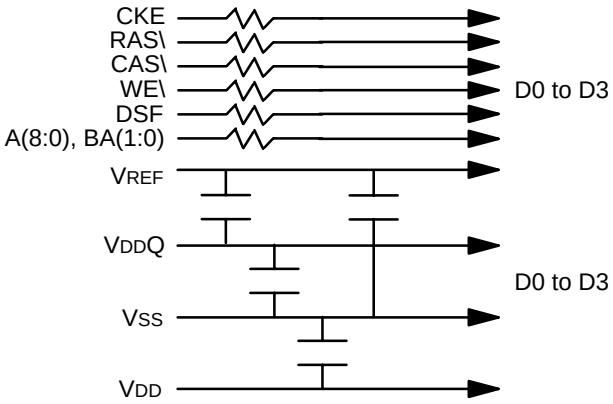


FIGURE 4.5.9–F
144 Pin, 512K X 2 Bank X 32 Configuration (4 MB)*





Series termination resistors are 28 W for double data rate lines (DQ, etc.) and 10 W for single data rate lines (CKE, etc.)



* This configuration can use 8 Mb DDR SGRAMs (256Kx32) for 4 MB total

FIGURE 4.5.9–G
144 Pin 1024K X 2 Bank X 32 Configuration (8 MB)*